



INTERNATIONAL  
CAMPUS OF  
EXCELLENCE

COORDINATION PROCESS OF  
LEARNING ACTIVITIES  
PR/CL/001



E.T.S. de Ingenieros  
Industriales

# ANX-PR/CL/001-01

## LEARNING GUIDE

### SUBJECT

**53001547 - Design Of Embedded Systems**

### DEGREE PROGRAMME

05BG - Master Universitario En Electronica Industrial

### ACADEMIC YEAR & SEMESTER

2019/20 - Semester 1

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## 1. Description

### 1.1. Subject details

Name of the subject	53001547 - Design Of Embedded Systems
No of credits	3 ECTS
Type	Optional
Academic year of the programme	First year
Semester of tuition	Semester 1
Tuition period	September-January
Tuition languages	English
Degree programme	05BG - Master Universitario En Electronica Industrial
Centre	05 - Escuela Tecnica Superior de Ingenieros Industriales
Academic year	2019-20

## 2. Faculty

### 2.1. Faculty members with subject teaching role

Name and surname	Office/Room	Email	Tutoring hours *
Jose Andres Otero Marnotes (Subject coordinator)	CEI	joseandres.oter0@upm.es	Sin horario. Disponible para tutorías cualquier día de la semana, en el horario de trabajo habitual. El horario de la tutoría será acordado vía email.

\* The tutoring schedule is indicative and subject to possible changes. Please check tutoring times with the faculty

member in charge.

## 2.2. Research assistants

Name and surname	Email	Faculty member in charge
Suriano , Leonardo	leonardo.suriano@upm.es	Otero Marnotes, Jose Andres

## 3. Prior knowledge recommended to take the subject

### 3.1. Recommended (passed) subjects

The subject - recommended (passed), are not defined.

### 3.2. Other recommended learning outcomes

- Digital Electronics, VHDL / Verilog
- Microcontroller Programming
- Microprocessor Architectures

## 4. Skills and learning outcomes \*

### 4.1. Skills to be learned

CB07 - Que los estudiantes sepan aplicar los conocimientos adquiridos y su capacidad de resolución de problemas en entornos nuevos o poco conocidos dentro de contextos más amplios (o multidisciplinares) relacionados con su área de estudio

CB09 - Que los estudiantes sepan comunicar sus conclusiones y los conocimientos y razones últimas que las sustentan a públicos especializados y no especializados de un modo claro y sin ambigüedades

CB10 - Que los estudiantes posean las habilidades de aprendizaje que les permitan continuar estudiando de un modo que habrá de ser en gran medida autodirigido o autónomo

CE01 - Comprender, diseñar y analizar sistemas y componentes electrónicos en el ámbito de la electrónica industrial. Modelización y caracterización de sistemas electrónicos complejos.

CE02 - Ser capaz de desarrollar un proyecto de diseño de un sistema electrónico, identificando sus principales

retos, en ámbitos de aplicación tales como el aeroespacial, la automoción, la ingeniería médica, las energías renovables o las comunicaciones

CE04 - Utilización de herramientas CAD para la simulación, modelado y diseño de circuitos electrónicos industriales con altas prestaciones y/o restricciones

CG01 - Haber adquirido conocimientos avanzados y demostrado, en un contexto de investigación científica y tecnológica o altamente especializado, una comprensión detallada y fundamentada de los aspectos teóricos y prácticos y de la metodología de trabajo en uno o más campos de estudio

CG02 - Saber aplicar e integrar sus conocimientos, la comprensión de estos, su fundamentación científica y sus capacidades de resolución de problemas en entornos nuevos y definidos de forma imprecisa, incluyendo contextos de carácter multidisciplinar tanto investigadores como profesionales altamente especializados.

CT01 - Uso de la lengua inglesa

CT02 - Liderazgo de equipos

CT03 - Creatividad

## 4.2. Learning outcomes

RA47 - Seleccionar y adaptar sistemas operativos embebidos y en tiempo real para la resolución de problemas concretos en el ámbito de los sistemas embebidos.

RA48 - Desarrollar soluciones de software embebido para la resolución de problemas concretos.

RA45 - Comprender las principales implicaciones del desarrollo de sistemas embebidos en diversos ámbitos, entre ellos, el aeroespacial.

RA46 - Construir sistemas embebidos empleando las herramientas de diseño adecuadas, tanto para el desarrollo de las plataformas hardware como el software asociado

\* The Learning Guides should reflect the Skills and Learning Outcomes in the same way as indicated in the Degree Verification Memory. For this reason, they have not been translated into English and appear in Spanish.

## 5. Brief description of the subject and syllabus

### 5.1. Brief description of the subject

This course tackles the problem of the design of embedded systems from a twofold point of view. On the one hand, it deals with hardware platforms for embedded systems on FPGAs, including on-chip communications, hardware/software interfaces, the implementation of custom accelerators and on-chip debugging techniques. On the other hand, Operating systems for embedded systems will be studied, since they are main components in nowadays systems. Special emphasis will be placed on real-time constraints. This course will have a practical orientation, based on the use of state-of-the art design tools (i.e. Xilinx Vivado), that enable the implementation of mixed systems with custom HW and the associated SW, that are implemented on state-of-the art SoPCs (i.e. Xilinx Zynq).

### 5.2. Syllabus

1. Embedded Computing Platforms
  - 1.1. System on Programmable Chips (SoPCs)
  - 1.2. On-chip Communications and Software/Hardware Interfaces
  - 1.3. Run-time SW/HW Debugging Techniques
2. Embedded Operating Systems
  - 2.1. Operating Systems Overview
  - 2.2. Embedded Linux for SoPCs
3. Real-Time Embedded Systems
  - 3.1. Real-time Systems & Scheduling
  - 3.2. Real-time Operating Systems: freeRTOS

## 6. Schedule

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### 6.1. Subject schedule\*

Week	Face-to-face classroom activities	Face-to-face laboratory activities	Other face-to-face activities	Assessment activities
1	<b>Introduction to Embedded System Design</b> Duration: 01:00  <b>System on Programmable Chip (SoPCs)</b> Duration: 02:00			
2		<b>Lab1: Basic SoPC Design with Vivado / Interrupts and Timers in Vivado</b> Duration: 03:00		<b>#Homework 1: Design of a System using Timers and Interrupts with Vivado</b>  Continuous assessment and final examination Duration: 03:00
3	<b>On-chip Communications and Hardware/Software Interfaces</b> Duration: 03:00			
4		<b>Lab 2: Custom IP Design and Integration with Vivado.</b> Duration: 03:00		
5	<b>Run-time SW/HW Debugging Techniques</b> Duration: 01:30	<b>Lab 3: SW/HW Debugging with VIVADO</b> Duration: 01:30		
6		<b>Lab 4: Performance Optimization using Direct Memory Access in SoPCs</b> Duration: 03:00		<b>#Homework 2: System Design with Custom IP wih Bare Metal Programming</b>  Continuous assessment and final examination Duration: 06:00
7	<b>Operating Systems Overview</b> Duration: 03:00			
8	<b>Embedded Linux for SoPCs</b> Duration: 02:00			
9		<b>Embedded Linux for Zynq (I)</b> Duration: 02:00		
10		<b>Embedded Linux for Zynq (II)</b> Duration: 02:00		

11	Real-time Systems & Scheduling Duration: 02:00			
12		FreeRTOS for Zynq Duration: 02:00		
13				Final Project: Complex HW/SW System design with VIVADO for Zynq  Continuous assessment and final examination Duration: 14:00
14				
15				
16				
17				Examen Final  Continuous assessment and final examination Duration: 02:00

The independent study hours are training activities during which students should spend time on individual study or individual assignments.

Depending on the programme study plan, total values will be calculated according to the ECTS credit unit as 26/27 hours of student face-to-face contact and independent study time.

\* The subject schedule is based on a previous theoretical planning of the subject plan and might go through some unexpected changes along throughout the academic year.

## 7. Activities and assessment criteria

### 7.1. Assessment activities

#### 7.1.1. Continuous assessment

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
2	#Homework 1: Design of a System using Timers and Interrupts with Vivado		No Presential	03:00	10%	5 / 10	
6	#Homework 2: System Design with Custom IP wih Bare Metal Programming		No Presential	06:00	10%	5 / 10	
13	Final Project: Complex HW/SW System design ith VIVADO for Zynq		No Presential	14:00	30%	5 / 10	CG02 CB10 CG01 CT02 CB09 CE04 CB07 CT01 CT03 CE01 CE02
17	Examen Final		Face-to-face	02:00	50%	5 / 10	

#### 7.1.2. Final examination

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
2	#Homework 1: Design of a System using Timers and Interrupts with Vivado		No Presential	03:00	10%	5 / 10	
6	#Homework 2: System Design with Custom IP wih Bare Metal Programming		No Presential	06:00	10%	5 / 10	
13	Final Project: Complex HW/SW System design ith VIVADO for Zynq		No Presential	14:00	30%	5 / 10	CG02 CB10 CG01 CT02 CB09 CE04 CB07 CT01 CT03 CE01

17	Examen Final		Face-to-face	02:00	50%	5 / 10	CE02
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### 7.1.3. Referred (re-sit) examination

No se ha definido la evaluación extraordinaria.

## 7.2. Assessment criteria

The evaluation of the course will be based on a final written exam (50% of the final mark, with a score of at least 5) and different practical assignments (50%) to be done by the students at home and in the lab, outside of the regular schedule for lectures. With the exam, the theoretical knowledge acquired by the students during the theoretical sessions will be evaluated. With the assignments, student must show their skills with Xilinx VIVADO and SDK, the CAD tools selected for the design of mixed HW/SW embedded systems, as well as with the Embedded Linux toolchain.

The Practical assignments will include a first short Homework to prove the basic skills with Vivado (10%) and a final complex project, dealing with the practical application of the embedded system design techniques studied throughout the course. This final project will be required in two different submissions. In the first one, the hardware implementation of the custom IP with bare metal programming will be evaluated (10% of the final mark). In the second one, the whole integrated project under an Embedded Linux support must be delivered.

## 8. Teaching resources

### 8.1. Teaching resources for the subject

Name	Type	Notes
Class Slides	Bibliography	Slides are delivered to the students in advance.
Pynq - Zynq Boards with custom shields	Equipment	These boards will be used for all VIVADO, SDK and Linux lab courses.
Introduction to Embedded Systems, A Cyber-Physical Systems Approach	Bibliography	Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, MIT Press, ISBN 978-0-262-53381-2, 2017.

A Practical Introduction to Hardware/Software Codesign	Bibliography	Patrick Schaumont, A Practical Introduction to Hardware/Software Codesign, Springer US, 2013
The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable Soc	Bibliography	Louise H. Crockett, Ross A. Elliot, Martin A. Enderwitz, Robert W. Stewart, The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable Soc, Strathclyde Academic Media, UK, 2014
Embedded Operating Systems A Practical Approach Series: Undergraduate Topics in Computer Science	Bibliography	A. Holt, C.-Y. Huang Embedded Operating Systems A Practical Approach Series: Undergraduate Topics in Computer Science, Springer-Verlag London, 978-1-4471-6602-3, 2014
Exploring Zynq® MPSoC With PYNQ and Machine Learning Applications	Bibliography	Louise H. Crockett, David Northcote, Craig Ramsay, Fraser D. Robinson, Robert W. Stewart, Department of Electronic & Electrical Engineering, University of Strathclyde, Glasgow, Scotland, UK., April 2019

## 9. Other information

### 9.1. Other information about the subject

The course has a deep practical approach. A good understanding of Verilog / VHDL description languages is required to be able to follow the course.