



POLITÉCNICA

INTERNATIONAL  
CAMPUS OF  
EXCELLENCE

COORDINATION PROCESS OF  
LEARNING ACTIVITIES  
PR/CL/001



E.T.S. de Ingenieros  
Industriales

# ANX-PR/CL/001-01

## LEARNING GUIDE

### SUBJECT

**53001549 - High Level Description Of Systems**

### DEGREE PROGRAMME

05BG - Master Universitario En Electronica Industrial

### ACADEMIC YEAR & SEMESTER

2019/20 - Semester 2

## Index

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### Learning guide

1. Description.....	1
2. Faculty.....	1
3. Prior knowledge recommended to take the subject.....	2
4. Skills and learning outcomes .....	2
5. Brief description of the subject and syllabus.....	4
6. Schedule.....	5
7. Activities and assessment criteria.....	7
8. Teaching resources.....	9

## 1. Description

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### 1.1. Subject details

<b>Name of the subject</b>	53001549 - High Level Description Of Systems
<b>No of credits</b>	3 ECTS
<b>Type</b>	Optional
<b>Academic year of the programme</b>	First year
<b>Semester of tuition</b>	Semester 2
<b>Tuition period</b>	February-June
<b>Tuition languages</b>	English
<b>Degree programme</b>	05BG - Master Universitario En Electronica Industrial
<b>Centre</b>	05 - Escuela Tecnica Superior de Ingenieros Industriales
<b>Academic year</b>	2019-20

## 2. Faculty

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### 2.1. Faculty members with subject teaching role

<b>Name and surname</b>	<b>Office/Room</b>	<b>Email</b>	<b>Tutoring hours *</b>
Jose Andres Otero Marnotes (Subject coordinator)		joseandres.otero@upm.es	Sin horario. Sin horario. Disponible para tutorías cualquier día de la semana, en el horario de trabajo habitual. El horario de la tutoria será acordado vía email.

\* The tutoring schedule is indicative and subject to possible changes. Please check tutoring times with the faculty member in charge.

## 2.2. Research assistants

Name and surname	Email	Faculty member in charge
Mariño Andres, Rodrigo	rodrigo.marino@upm.es	Otero Marnotes, Jose Andres

## 3. Prior knowledge recommended to take the subject

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### 3.1. Recommended (passed) subjects

- Integrated Circuits And Reconfigurable Computing
- Design Of Embedded Systems
- Electronic Lab

### 3.2. Other recommended learning outcomes

- VHDL / Verilog
- Basic programming
- Digital system design

## 4. Skills and learning outcomes \*

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### 4.1. Skills to be learned

CB07 - Que los estudiantes sepan aplicar los conocimientos adquiridos y su capacidad de resolución de problemas en entornos nuevos o poco conocidos dentro de contextos más amplios (o multidisciplinares) relacionados con su área de estudio

CB08 - Que los estudiantes sean capaces de integrar conocimientos y enfrentarse a la complejidad de formular juicios a partir de una información que, siendo incompleta o limitada, incluya reflexiones sobre las responsabilidades sociales y éticas vinculadas a la aplicación de sus conocimientos y juicios

CB09 - Que los estudiantes sepan comunicar sus conclusiones y los conocimientos y razones últimas que las

sustentan a públicos especializados y no especializados de un modo claro y sin ambigüedades

CE01 - Comprender, diseñar y analizar sistemas y componentes electrónicos en el ámbito de la electrónica industrial. Modelización y caracterización de sistemas electrónicos complejos.

CE04 - Utilización de herramientas CAD para la simulación, modelado y diseño de circuitos electrónicos industriales con altas prestaciones y/o restricciones

CG01 - Haber adquirido conocimientos avanzados y demostrado, en un contexto de investigación científica y tecnológica o altamente especializado, una comprensión detallada y fundamentada de los aspectos teóricos y prácticos y de la metodología de trabajo en uno o más campos de estudio

CG03 - Saber evaluar y seleccionar la teoría científica adecuada y la metodología precisa de sus campos de estudio para formular juicios a partir de información incompleta o limitada incluyendo, cuando sea preciso y pertinente, una reflexión sobre la responsabilidad social o ética ligada a la solución que se proponga en cada caso.

CT03 - Creatividad

## 4.2. Learning outcomes

RA15 - Distinguir los resultados obtenidos a partir de diferentes lenguajes, como SystemC y VHDL

RA16 - Interpretar y juzgar la complejidad de un sistema y seleccionar la herramienta de diseño más apropiada

RA14 - Utilizar herramientas específicas para el diseño y simulación de circuitos integrados.

\* The Learning Guides should reflect the Skills and Learning Outcomes in the same way as indicated in the Degree Verification Memory. For this reason, they have not been translated into English and appear in Spanish.

## 5. Brief description of the subject and syllabus

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### 5.1. Brief description of the subject

This course is intended to introduce the students into system-level design techniques and optimization of hardware implementation of digital electronic systems.

The topics covered in the subject go from the languages and tools for system-level design to the implementation of accelerators using high-level synthesis from algorithmic descriptions.

The practical part will be done using Xilinx tools like Vivado HLS and implementation in SoPC like ZynQ.

### 5.2. Syllabus

1. Course Overview
2. High-Level Synthesis of Algorithms
  - 2.1. Introduction to Algorithmic Synthesis
  - 2.2. Design Space Exploration and Trade-offs
  - 2.3. General Procedure: Scheduling, Binding and Mapping
  - 2.4. Hardware Optimizations with HLS
  - 2.5. Tutorials with Vivado HLS
3. System-level Design and Validation
  - 3.1. System Level Design with SystemC
  - 3.2. Hardware / Software Codesign
  - 3.3. Tutorials with SystemC

## 6. Schedule

### 6.1. Subject schedule\*

Week	Face-to-face classroom activities	Face-to-face laboratory activities	Other face-to-face activities	Assessment activities
1	<b>Course Overview</b> Duration: 01:00  <b>Introduction to Algorithmic Synthesis</b> Duration: 01:00			
2	<b>Design Space Exploration and Trade-offs</b> Duration: 02:00			
3	<b>General Procedure: Scheduling, Binding and Mapping</b> Duration: 02:00			<b>Homework of Scheduling, Allocation and Binding</b>  Continuous assessment and final examination Duration: 04:00
4	<b>General Procedure: Scheduling, Binding and Mapping</b> Duration: 01:00  <b>A Bird's Eye on Vivado HLS</b> Duration: 01:00			
5		<b>Lab 1: Custom IP Design and Integration with Vivado HLS</b> Duration: 02:00		
6	<b>Hardware Optimizations with HLS</b> Duration: 02:00			
7		<b>Lab 2: Advanced Design of Accelerators with Vivado HLS</b> Duration: 03:00		
8		<b>Lab 3: Optimizations with Vivado HLS</b> Duration: 03:00		<b>Homework of HLS</b>  Continuous assessment and final examination Duration: 02:00
9	<b>Model-based Design</b> Duration: 01:00	<b>Lab 4: Model-based Design with Matlab / Simulink</b> Duration: 02:00		<b>Homework of Hardware Design with Simulink</b>  Continuous assessment and final examination Duration: 04:00

10	<b>System-Level Design with SystemC</b> Duration: 03:00			
11		<b>Lab5: Introduction to SystemC</b> Duration: 03:00		
12		<b>Lab 6: Software / Hardware Partitioning with SystemC</b> Duration: 03:00		<b>Homework of SystemC</b>  Continuous assessment and final examination Duration: 04:00
13				
14				
15				
16				<b>Final Exam</b>  Continuous assessment and final examination Duration: 02:00
17				

The independent study hours are training activities during which students should spend time on individual study or individual assignments.

Depending on the programme study plan, total values will be calculated according to the ECTS credit unit as 26/27 hours of student face-to-face contact and independent study time.

\* The subject schedule is based on a previous theoretical planning of the subject plan and might go through experience some unexpected changes along throughout the academic year.



## 7. Activities and assessment criteria

### 7.1. Assessment activities

#### 7.1.1. Continuous assessment

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
3	Homework of Scheduling, Allocation and Binding		No Presential	04:00	5%	5 / 10	
8	Homework of HLS		Face-to-face	02:00	25%	5 / 10	CB07 CB08 CT03 CE04 CE01
9	Homework of Hardware Design with Simulink		Face-to-face	04:00	10%	5 / 10	
12	Homework of SystemC		Face-to-face	04:00	20%	5 / 10	
16	Final Exam		No Presential	02:00	40%	5 / 10	CB08 CT03 CE04 CG01 CG03 CB09 CE01 CB07

#### 7.1.2. Final examination

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
3	Homework of Scheduling, Allocation and Binding		No Presential	04:00	5%	5 / 10	
8	Homework of HLS		Face-to-face	02:00	25%	5 / 10	CB07 CB08 CT03 CE04 CE01
9	Homework of Hardware Design with Simulink		Face-to-face	04:00	10%	5 / 10	
12	Homework of SystemC		Face-to-face	04:00	20%	5 / 10	

16	Final Exam		No Presential	02:00	40%	5 / 10	CB08 CT03 CE04 CG01 CG03 CB09 CE01 CB07
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### 7.1.3. Referred (re-sit) examination

No se ha definido la evaluación extraordinaria.

## 7.2. Assessment criteria

This subject will be evaluated based on the following aspects:

1. a homework problem that the students will have to provide and discuss in the class (individual)
2. a practical work implementing Different Algorithms by means of High Level Synthesis Tools (team work)
3. a practical work implementing a simple Algorithm by means of Simulink (team work)
4. a practical work modeling a basic Software / Hardware System with SystemC (team work)
5. A Final Exam covering the whole subject (individual)

## 8. Teaching resources

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### 8.1. Teaching resources for the subject

Name	Type	Notes
Papers	Bibliography	
Xilinx Tools (Vivado)	Equipment	
PynQ boards	Equipment	
slides for the classes	Bibliography	