ANX-PR/CL/001-01

LEARNING GUIDE

SUBJECT

593000427 - Embedded Systems

DEGREE PROGRAMME

59AG - Eit Digital Track On Internet Technology And Architecture

ACADEMIC YEAR & SEMESTER

2020/21 - Semester 2

Index

Learning guide

1. Description

1.1. Subject details

Name of the subject	593000427 - Embedded Systems
No of credits	5 ECTS
Type	Optional
Academic year ot the programme	First year
Semester of tuition	Semester 2
Tuition period	February-June
Tuition languages	English
Degree programme	59AG - Eit Digital Track On Internet Technology And Architecture
Centre	59 - Escuela Tecnica Superior de Ingenieria y Sistemas de Telecomunicacion
Academic year	2020-21

2. Faculty

2.1. Faculty members with subject teaching role

Name and surname	Office/Room	Email	Tutoring hours *
Cesar Sanz Alvaro	A6104	cesar.sanz@upm.es	W - 16:30 - 17:30
Eduardo Juarez Martinez (Subject coordinator)	A4204	eduardo.juarez@upm.es	W - 16:30 - 17:30
Antonio Carpeño Ruiz	A4219	antonio.cruiz@upm.es	W - 16:30 - 17:30

* The tutoring schedule is indicative and subject to possible changes. Please check tutoring times with the faculty member in charge.

3. Prior knowledge recommended to take the subject

3.1. Recommended (passed) subjects

- Advanced Digital Architectures

3.2. Other recommended learning outcomes

- Programming and debugging using the C language (with emphasis on structures, pointers and memory management)

- Application of processor peripherals

- Application of processor interrupts

- Application of the Von Neumann's computer architecture

- Analysis, application and design of wired digital circuits

4. Skills and learning outcomes *

4.1. Skills to be learned

CB.6 - To have knowledge that provides the basis or the opportunity of being original to develop and/or to apply ideas, usually in a research context

CB.10 - To be capable of applying the students' acquired knowledge, as well as their problem solving abilities, to new or not well-knownTo have the learning abilities to continue studying in a mostly self-guided or autonomous manner

CB.7 - To be capable of applying the students' acquired knowledge, as well as their problem solving abilities, to new or not well-known environments in broader (or multidisciplinary) contexts that are in the framework of their expertise area.

CE.1 - To be capable of analyzing, interpreting and applying standards related to the ICT

CE.7 - To be capable of proposing, organizing and executing research works in the framework of the Information Society engineering.

CESI.3 - To be capable of analyzing and developing embedded systems integrating operating systems.

CESI.4 - To be capable of developing systems which are based on programmable devices.

CGEN.3 - To be capable of elaborating, planning strategically, leading, coordinating and managing, both technically and economically, projects in the framework of the Information Society engineering, according to ethical, quality and environmental criteria.

CGEN.4 - To be capable of planning, calculating and designing systems and services for the Information Society.

4.2. Learning outcomes

RA12 - Develop synthesizable VHDL models for combinational and sequential synchronous circuits

RA17 - Analyze and evaluate the operating systems deployable in an embedded system

RA13 - Deploy an operating system in an embedded processor

RA14 - Develop VHDL structural descriptions of digital systems

RA15 - Shape the hardware architecture of a digital system

RA16 - Apply the simulation and synthesis tools of a CAD environment

RA11 - Analyze embedded systems, the technologies needed by them and the theoretical foundations for their systematic design

RA18 - Develop test-benches and simulate them in a VHDL simulator

* The Learning Guides should reflect the Skills and Learning Outcomes in the same way as indicated in the Degree Verification Memory. For this reason, they have not been translated into English and appear in Spanish.

5. Brief description of the subject and syllabus

5.1. Brief description of the subject

This course is a continuation of the Advanced Digital Architecture (ADA) course. While two of the technologies to implement an embedded system are taught in ADA, the third one, FPGA, is covered here. The course begins with the basics of Programmable Logic Devices (PLD) as a target technology. Then, the VHDL language is applied to model two types of hierarchical digital subsystems: combinational and sequential. At last, in this block, VHDL test-bench specifications and stimuli are explained, applied and implemented. A complex VHDL test-bench specification is proposed as use-case to exercise the previous concepts.

Next block begins covering the architecture of current configurable embedded processors and the hardware design flow to synthesize the architecture of an embedded system. Afterwards, the software structure of an OS driver aimed to manage a custom-made peripheral is presented. At last, as a use-case, the student implements an embedded system consisting of a configurable embedded processor with a custom-made peripheral and its corresponding software.

5.2. Syllabus

1. Programmable Logic Devices
2. VHDL Language
3. Functional Verification and Test-Bench Design
4. Configurable Embedded Systems
5. Software Design Flow for Embedded Systems
6. Course Project

6. Schedule

6.1. Subject schedule*

Week	Face-to-face classroom activities	Face-to-face laboratory activities	Distant / On-line	Assessment activities
1	**Course Introduction** Duration: 00:45 **Lesson 1: Programmable Logic Devices Review** Duration: 02:15			**Lesson 1. Assessment of the proposed exercise** Continuous assessment Not Presential Duration: 00:15
2	**Lesson 2: Designing with Hardware Description Languages (HDL)** Duration: 00:30 **Lesson 2: VHDL Language** Duration: 01:30	**Lesson 2: Design flow for VHDL models using CAD tools** Duration: 00:45		**Lesson 2. Hands-on exercises to assess Modelsim profiency** Continuous assessment Presential Duration: 00:15 **Lesson 2. Assesment of the implementation and test-bench of some example circuits** Continuous assessment Not Presential Duration: 00:15
3	**Lesson 2: VHDL Language** Duration: 03:00			
4	**Lesson 3. VHDL language syntax for functional verification. Test-bench design** Duration: 03:00			**Lesson 3. Assesment of the proposed exercises** Continuous assessment Not Presential Duration: 00:15
5		**Lesson 3: Design of the test-bench of a simple given entity using signal generation, procedures and complex stimuli** Duration: 03:00		**Lesson 3. Assesment of the design of the test-bench of a simple given entity using signal generation, procedures and complex stimuli** Continuous assessment Not Presential Duration: 00:15
6	**Lesson 4: Concept of Configurable Embedded System. Current Configurable Embedded Systems** Duration: 03:00			

7	**Lesson 4: Case-Study of Cyclone V SOC** Duration: 03:00			
8		**Lesson 4: Synthesis of a Given Configurable Embedded System Architecture on a FPGA-based board** Duration: 03:00		**Lesson 4. Assesment of the synthesis of a given configurable embedded system architecture on a FPGA-based board.** Continuous assessment Not Presential Duration: 00:15
9	**Lesson 5: Fundamentals of Linux Driver Development. The structure of a Linux Driver Module** Duration: 03:00			
10	**Lesson 5: Case-Study. Linux kernel support for inter-context data exchange, memory allocation, synchronization, timing, hw communication and interrupt management** Duration: 03:00			
11		**Lesson 5. Tutorial: deploying a Embedded Linux OS on a configurable embedded system using a SoC** Duration: 03:00		
12		**Lesson 5. Tutorial: deploying a Embedded Linux OS on a configurable embedded system using a SoC** Duration: 03:00		**Lesson 5. Assessment of the deployment of a linux OS on a configurable embedded system with a device driver** Continuous assessment Not Presential Duration: 00:15
13		**Lesson 6: Course Project** Duration: 03:00		
14		**Lesson 6: Course Project** Duration: 03:00		
15				
16				
				Lesson 3 (solo prueba final) Final examination Not Presential Duration: 00:15 **Lesson 6. Assesment of the synthesis of an embedded system comprising a configurable embedded processor with a custom made peripheral and its accompaning software to fit a given application** Continuous assessment Presential Duration: 02:00 **Lesson 6 (solo prueba final)**

17				Final examination Not Presential Duration: 00:15 **Practice exam Lessons 3 and 6 (solo prueba final)** Final examination Presential Duration: 01:30 **Oral exam (solo prueba final)** Final examination Presential Duration: 02:00 **Written exam Lessons 3 and 6 (solo prueba final)** Final examination Presential Duration: 01:30

Depending on the programme study plan, total values will be calculated according to the ECTS credit unit as 26/27 hours of student face-to-face contact and independent study time.

* The schedule is based on an a priori planning of the subject; it might be modified during the academic year, especially considering the COVID19 evolution.

7. Activities and assessment criteria

7.1. Assessment activities

7.1.1. Continuous assessment

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
1	Lesson 1. Assessment of the proposed exercise		No Presential	00:15	5%	5 / 10	CESI.3
2	Lesson 2. Hands-on exercises to assess Modelsim profiency		Face-to-face	00:15	5%	5 / 10	CESI.3
2	Lesson 2. Assesment of the implementation and test-bench of some example circuits		No Presential	00:15	5%	5 / 10	CESI.3
4	Lesson 3. Assesment of the proposed exercises		No Presential	00:15	10%	5 / 10	CESI.3
5	Lesson 3. Assesment of the design of the test-bench of a simple given entity using signal generation, procedures and complex stimuli		No Presential	00:15	20%	5 / 10	CE.1 CESI.3 CB.6
8	Lesson 4. Assesment of the synthesis of a given configurable embedded system architecture on a FPGA-based board.		No Presential	00:15	5%	5 / 10	CESI.4
12	Lesson 5. Assessment of the deployment of a linux OS on a configurable embedded system with a device driver		No Presential	00:15	5%	5 / 10	CESI.4
17	Lesson 6. Assesment of the synthesis of an embedded system comprising a configurable embedded processor with a custom made peripheral and its accompaning software to fit a given application		Face-to-face	02:00	45%	5 / 10	CB.10 CE.1 CGEN.4 CE.7 CESI.4 CGEN.3 CB.7 CB.6

7.1.2. Final examination

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills

17	Lesson 3 (solo prueba final)		No Presential	00:15	20%	5 / 10	CESI.3
17	Oral exam (solo prueba final)		Face-to-face	02:00	20%	5 / 10	CB.10 CE.1 CESI.3 CGEN.4 CE.7 CESI.4 CGEN.3 CB.7 CB.6
17	Lesson 6 (solo prueba final)		No Presential	00:15	20%	5 / 10	CESI.4
17	Practice exam Lessons 3 and 6 (solo prueba final)		Face-to-face	01:30	20%	5 / 10	CB.10 CE.1 CESI.3 CGEN.4 CE.7 CESI.4 CGEN.3 CB.7 CB.6
17	Written exam Lessons 3 and 6 (solo prueba final)		Face-to-face	01:30	20%	5 / 10	CESI.3 CB.10 CE.1 CGEN.4 CE.7 CESI.4 CGEN.3 CB.7 CB.6

7.1.3. Referred (re-sit) examination

Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
Lesson 3		Face-to-face	00:15	20%	5 / 10	CESI.3
Lesson 6		Face-to-face	00:15	20%	5 / 10	CESI.4
Practice exam Lessons 3 and 6		Face-to-face	01:30	20%	5 / 10	CESI.3 CGEN.4 CE.7 CESI.4 CGEN.3 CB.10 CE.1 CB.7

						CB.6
Oral exam		Face-to-face	02:00	20%	5 / 10	CB.10 CE.1 CESI.3 CGEN.4 CE.7 CESI.4 CGEN.3 CB.7 CB.6
Written exam Lesson 3 and 6		Face-to-face	01:30	20%	5 / 10	CB.10 CE.1 CESI.3 CGEN.4 CE.7 CESI.4 CGEN.3 CB.7 CB.6

7.2. Assessment criteria

The Master's program to which this subject belongs has entered its termination phase. There will be only "Solo Prueba Final" Assessment

"Solo Prueba Final" Assessment

The "Solo Prueba Final" assessment will consist of the following components:

- Project I (lesson 3): simple peripheral verification
- Project II (lesson 6): synthesis of an embedded system comprising a configurable embedded processor
- Exam of projects I and II: it is a written and practice exam of the projects I and II

- Oral exam about the exercises proposed along the course

The grade will be composed of the following elements:

- Assessment of project I: 20% (2 points)
- Assessment of project II: 20% (2 points)
- Exam of projects I and II: 40% (4 points)
- Oral exam: 20% (2 points)

In each of the elements, a grade greater than or equal to 5.0 points is required

The "Examen Extraordinario" assesment will consist of the same components and weights as those of the "Solo Prueba Final" assessment

8. Teaching resources

8.1. Teaching resources for the subject

Name	Type	Notes
VHDL for Logic Synthesis	Bibliography	Andrew Rushton Wiley; 2 edition (July 7, 1998) 390 pages ISBN: 978-0471983255
The Design Warrior?s Guide to	Bibliography	Clive Maxfield Elsevier; 2004 542 pages ISBN: 978-0750676045

Altera Cyclone V SoC Literature	Web resource	Freely downloadable from Altera?s web page at http://www.altera.com
Linux Device Drivers, 3rd edition	Bibliography	Jonathan Corbet, Alessandro Rubini & Greg Kroah-Hartman O'Reilly Media; 3 edition (February 7, 2005) 640 pages ISBN: 978-0596005900 Freely downloadable from http://lw.net/Kernel/LDD3