ANX-PR/CL/001-01

LEARNING GUIDE

SUBJECT

53001548 - Embedded Processing Architectures

DEGREE PROGRAMME

05BG - Master Universitario En Electronica Industrial

ACADEMIC YEAR & SEMESTER

2021/22 - Semester 2

Index

Learning guide

1. Description

1.1. Subject details

Name of the subject	53001548 - Embedded Processing Architectures
No of credits	3 ECTS
Type	Optional
Academic year ot the programme	First year
Semester of tuition	Semester 2
Tuition period	February-June
Tuition languages	English
Degree programme	05BG - Master Universitario en Electronica Industrial
Centre	05 - Escuela Tecnica Superior De Ingenieros Industriales
Academic year	2021-22

2. Faculty

2.1. Faculty members with subject teaching role

Name and surname	Office/Room	Email	Tutoring hours *
Alfonso Rodriguez Medina (Subject coordinator)	UD Electrónica	alfonso.rodriguezm@upm.es	Sin horario. Please send an email to arrange a meeting

* The tutoring schedule is indicative and subject to possible changes. Please check tutoring times with the faculty member in charge.

3. Prior knowledge recommended to take the subject

3.1. Recommended (passed) subjects

The subject - recommended (passed), are not defined.

3.2. Other recommended learning outcomes

- Generic knowledge of microprocessor/microcontroller programming

- Basic computer architecture background

4. Skills and learning outcomes *

4.1. Skills to be learned

CB06 - Poseer y comprender conocimientos que aporten una base u oportunidad de ser originales en el desarrollo y/o aplicación de ideas, a menudo en un contexto de investigación

CB07 - Que los estudiantes sepan aplicar los conocimientos adquiridos y su capacidad de resolución de problemas en entornos nuevos o poco conocidos dentro de contextos más amplios (o multidisciplinares) relacionados con su área de estudio

CB08 - Que los estudiantes sean capaces de integrar conocimientos y enfrentarse a la complejidad de formular juicios a partir de una información que, siendo incompleta o limitada, incluya reflexiones sobre las responsabilidades sociales y éticas vinculadas a la aplicación de sus conocimientos y juicios

CE01 - Comprender, diseñar y analizar sistemas y componentes electrónicos en el ámbito de la electrónica industrial. Modelización y caracterización de sistemas electrónicos complejos.

CG01 - Haber adquirido conocimientos avanzados y demostrado, en un contexto de investigación científica y tecnológica o altamente especializado, una comprensión detallada y fundamentada de los aspectos teóricos y prácticos y de la metodología de trabajo en uno o más campos de estudio

CG02 - Saber aplicar e integrar sus conocimientos, la comprensión de estos, su fundamentación científica y sus capacidades de resolución de problemas en entornos nuevos y definidos de forma imprecisa, incluyendo contextos de carácter multidisciplinar tanto investigadores como profesionales altamente especializados.

CG06 - Haber desarrollado la autonomía suficiente para participar en proyectos de investigación y colaboraciones científicas o tecnológicas dentro de su ámbito temático, en contextos interdisciplinares y, en su caso, con una alta componente de transferencia del conocimiento.

CT01 - Uso de la lengua inglesa

4.2. Learning outcomes

RA25 - Saber clasificar las arquitecturas y modelos de computación para el caso de los sistemas multicore y los manycore.

RA26 - Aplicar criterios de valoración y de selección de las opciones óptimas para resolver problemas de cómputo complejos, empleando arquitecturas de procesamiento avanzadas.

RA24 - Aplicar e integrar los conocimientos sobre diseño de sistemas microprocesadores avanzados y de procesamiento paralelo

* The Learning Guides should reflect the Skills and Learning Outcomes in the same way as indicated in the Degree Verification Memory. For this reason, they have not been translated into English and appear in Spanish.

5. Brief description of the subject and syllabus

5.1. Brief description of the subject

This subject is focused as an architectural approach towards more performing processing architectures. Nowadays, there is a paradigmatic change from single processing architectures to multiple processor / multiple core approaches. There is no way to increase performance with just a single core, and so, other alternatives are required.

We are assuming students have basic knowledge of microprocessor programming and basic architectures. Taking this as the starting point, we first review ways of improving performance by means of enhanced architectures, improved from the point of view of internal bus arrangements, load/store operation, RISC instruction set coding, and, later, pipelining and memory hierarchy are reviewed in detailed. All these approaches are done quantitatively and trading cost vs performance (following the world widespread theories from Patterson and Hennesy),

Once it is shown that there are no further ways to improve performance with single core architectures, we move to multi core and many core approaches. Here, the problem is not only architectural, but also it has an impact on how to program and synchronize this type of systems. Therefore, this part contains an interleaved scheme where architectures are reviewed and then, ways of programming them are explained and practiced.

To this regard, then multi-core (shred memory or distributed memory) approaches are seen, and programming with pthreads and OpenMP is done in a mixed practical class approach, with a work afterwards. Then, other models of computation such as the dataflow model are seen, and an academic tool to convert dataflow-based programs into ptherad multicore schemes is used. The third part within this parallel processing area is many core systems, such as GPGPUs. Again, the GPGPU architecture is presented, followed by CUDA/OpenCL practical classes.

5.2. Syllabus

1. Microprocessor architectures
    1.1. Cost vs performance trade-offs
    1.2. Single core architectures. Evolution
    1.3. Segmented (pieplined) architectures
    1.4. Memory hierarchy
2. Parallel architectures
    2.1. Cost/performance issues in parallel architectures
    2.2. Parallel computing models
    2.3. ptheads and OpenMP programming
    2.4. Distributed Programming
    2.5. MPI Programming
    2.6. Dataflow models of computation
    2.7. GPGPU architectures
    2.8. OpenCL/CUDA programming

6. Schedule

6.1. Subject schedule*

Week	Face-to-face classroom activities	Face-to-face laboratory activities	Distant / On-line	Assessment activities
1	**Cost vs performance** Duration: 02:00			**Projects** Continuous assessment and final examination Presential Duration: 20:00 **Homework** Continuous assessment and final examination Presential Duration: 10:00
2	**Single core architectures** Duration: 02:00			
3	**Segmented (pipelined) architectures** Duration: 02:00			
4	**Memory hierarchy/caches** Duration: 02:00			
5	**Cost/performance in parallel architectures** Duration: 02:00			
6	**Parallel computing models** Duration: 02:00			
7		**pthreads and OpenMP programming** Duration: 03:00		
8	**Dsitributed programming** Duration: 03:00			
9		**MPI: Message Passing Interface Programming** Duration: 03:00		
10		**Dataflow computing. PREESM tool** Duration: 03:00		

11	**GPGPU Architecture** Duration: 03:00			
12		**OpenCL/CUDA Programming** Duration: 03:00		
13				
14				
15				**Exam** Continuous assessment and final examination Presential Duration: 02:00
16				
17				

Depending on the programme study plan, total values will be calculated according to the ECTS credit unit as 26/27 hours of student face-to-face contact and independent study time.

* The schedule is based on an a priori planning of the subject; it might be modified during the academic year, especially considering the COVID19 evolution.

7. Activities and assessment criteria

7.1. Assessment activities

7.1.1. Continuous assessment

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
1	Projects		Face-to-face	20:00	40%	5 / 10	CG06 CB06 CB07 CT01 CE01
1	Homework		Face-to-face	10:00	10%	5 / 10	
15	Exam		Face-to-face	02:00	50%	5 / 10	CG01 CG02 CB08

7.1.2. Final examination

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
1	Projects		Face-to-face	20:00	40%	5 / 10	CG06 CB06 CB07 CT01 CE01
1	Homework		Face-to-face	10:00	10%	5 / 10	
15	Exam		Face-to-face	02:00	50%	5 / 10	CG01 CG02 CB08

7.1.3. Referred (re-sit) examination

No se ha definido la evaluación extraordinaria.

7.2. Assessment criteria

The score is based on:

Final exam - 50%
Practical projects - 40%
Homework - 10%

8. Teaching resources

8.1. Teaching resources for the subject

Name	Type	Notes
Bibliography	Bibliography	Computer Architecture: A Quantitative Approach (6th Edition). John Hennessy & David Patterson.