



INTERNATIONAL  
CAMPUS OF  
EXCELLENCE

COORDINATION PROCESS OF  
LEARNING ACTIVITIES  
PR/CL/001



E.T.S. de Ingenieros  
Industriales

# ANX-PR/CL/001-01

## LEARNING GUIDE

### SUBJECT

**53001549 - High Level Description Of Systems**

### DEGREE PROGRAMME

05BG - Master Universitario En Electronica Industrial

### ACADEMIC YEAR & SEMESTER

2021/22 - Semester 2

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## 1. Description

### 1.1. Subject details

Name of the subject	53001549 - High Level Description Of Systems
No of credits	3 ECTS
Type	Optional
Academic year of the programme	First year
Semester of tuition	Semester 2
Tuition period	February-June
Tuition languages	English
Degree programme	05BG - Master Universitario en Electronica Industrial
Centre	05 - Escuela Técnica Superior De Ingenieros Industriales
Academic year	2021-22

## 2. Faculty

### 2.1. Faculty members with subject teaching role

Name and surname	Office/Room	Email	Tutoring hours *
Jose Andres Otero Marnotes (Subject coordinator)		joseandres.oter@upm.es	Sin horario. Sin horario. Disponible para tutorías cualquier día de la semana, en el horario de trabajo habitual. El horario de la tutoría será acordado vía email.

\* The tutoring schedule is indicative and subject to possible changes. Please check tutoring times with the faculty member in charge.

### 3. Prior knowledge recommended to take the subject

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#### 3.1. Recommended (passed) subjects

- Integrated Circuits And Reconfigurable Computing
- Design Of Embedded Systems
- Electronic Lab

#### 3.2. Other recommended learning outcomes

- VHDL / Verilog
- Basic programming
- Digital system design
- C/C++

### 4. Skills and learning outcomes \*

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#### 4.1. Skills to be learned

CB07 - Que los estudiantes sepan aplicar los conocimientos adquiridos y su capacidad de resolución de problemas en entornos nuevos o poco conocidos dentro de contextos más amplios (o multidisciplinares) relacionados con su área de estudio

CB08 - Que los estudiantes sean capaces de integrar conocimientos y enfrentarse a la complejidad de formular juicios a partir de una información que, siendo incompleta o limitada, incluya reflexiones sobre las responsabilidades sociales y éticas vinculadas a la aplicación de sus conocimientos y juicios

CB09 - Que los estudiantes sepan comunicar sus conclusiones y los conocimientos y razones últimas que las sustentan a públicos especializados y no especializados de un modo claro y sin ambigüedades

CE01 - Comprender, diseñar y analizar sistemas y componentes electrónicos en el ámbito de la electrónica

industrial. Modelización y caracterización de sistemas electrónicos complejos.

CE04 - Utilización de herramientas CAD para la simulación, modelado y diseño de circuitos electrónicos industriales con altas prestaciones y/o restricciones

CG01 - Haber adquirido conocimientos avanzados y demostrado, en un contexto de investigación científica y tecnológica o altamente especializado, una comprensión detallada y fundamentada de los aspectos teóricos y prácticos y de la metodología de trabajo en uno o más campos de estudio

CG03 - Saber evaluar y seleccionar la teoría científica adecuada y la metodología precisa de sus campos de estudio para formular juicios a partir de información incompleta o limitada incluyendo, cuando sea preciso y pertinente, una reflexión sobre la responsabilidad social o ética ligada a la solución que se proponga en cada caso.

CT03 - Creatividad

## 4.2. Learning outcomes

RA15 - Distinguir los resultados obtenidos a partir de diferentes lenguajes, como SystemC y VHDL

RA16 - Interpretar y juzgar la complejidad de un sistema y seleccionar la herramienta de diseño más apropiada

RA14 - Utilizar herramientas específicas para el diseño y simulación de circuitos integrados.

\* The Learning Guides should reflect the Skills and Learning Outcomes in the same way as indicated in the Degree Verification Memory. For this reason, they have not been translated into English and appear in Spanish.

## 5. Brief description of the subject and syllabus

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### 5.1. Brief description of the subject

This course is intended to introduce the students into system-level design techniques and optimization of hardware implementation of digital electronic systems.

The topics covered in the subject go from the languages and tools for system-level design to the implementation of accelerators using high-level synthesis from algorithmic descriptions.

The practical part will be done using Xilinx tools like Vivado HLS and implementation in SoPC like ZynQ. We will also use a specific C++ compiler for SystemC descriptions.

## 5.2. Syllabus

1. Course Overview
2. High-Level Synthesis of Algorithms
  - 2.1. Introduction to Algorithmic Synthesis
  - 2.2. General Procedure: Scheduling, Binding and Mapping
  - 2.3. Design Space Exploration and Trade-offs
  - 2.4. Hardware Optimizations with HLS
  - 2.5. Tutorials with Vivado HLS
3. Model-Based Design
  - 3.1. Model-Based Design Principles
  - 3.2. Tutorials of Model Based Design with Simulink
4. System-level Design and Validation
  - 4.1. Hardware / Software Codesign
  - 4.2. System Level Design with SystemC
  - 4.3. Tutorials with SystemC

## 6. Schedule

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### 6.1. Subject schedule\*

Week	Face-to-face classroom activities	Face-to-face laboratory activities	Distant / On-line	Assessment activities
1	<b>Course Overview</b> Duration: 01:00  <b>Introduction to Algorithmic Synthesis</b> Duration: 01:00			
2	<b>Scheduling, Binding and Mapping</b> Duration: 02:00			
3	<b>Scheduling, Binding and Mapping</b> Duration: 02:00			Homework of Scheduling, Allocation and Binding  Continuous assessment and final examination Not Presential Duration: 04:00
4	<b>Design Space Exploration and Trade-offs</b> Duration: 02:00			
5	<b>Hardware Optimizations with HLS</b> Duration: 02:00			
6		<b>Lab 1: Introduction to Vivado HLS</b> Duration: 02:00		
7		<b>Lab 2: Design Optimization in Vivado HLS</b> Duration: 02:00		
8		<b>Lab 3: Optimizing Matrix Multiplications in Vivado HLS</b> Duration: 02:00		Homework of HLS  Continuous assessment and final examination Presential Duration: 06:00
9	<b>Model-based Design</b> Duration: 02:00			
10		<b>Lab 4: Model-based Design with Matlab / Simulink</b> Duration: 02:00		Homework of Hardware Design with Simulink  Continuous assessment and final examination Presential Duration: 04:00

11	<b>System-Level Design with SystemC</b> Duration: 02:00			
12	<b>Hardware / Software Codesign</b> Duration: 02:00			
13		<b>Lab5: Introduction to SystemC</b> Duration: 02:00		
14		<b>Lab 6: Software / Hardware Partitioning with SystemC</b> Duration: 02:00		<b>Homework of SystemC</b>  Continuous assessment and final examination Presential Duration: 06:00
15				<b>Final Exam</b>  Continuous assessment and final examination Not Presential Duration: 02:00
16				
17				

Depending on the programme study plan, total values will be calculated according to the ECTS credit unit as 26/27 hours of student face-to-face contact and independent study time.

\* The schedule is based on an a priori planning of the subject; it might be modified during the academic year, especially considering the COVID19 evolution.

## 7. Activities and assessment criteria

### 7.1. Assessment activities

#### 7.1.1. Continuous assessment

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
3	Homework of Scheduling, Allocation and Binding		No Presential	04:00	5%	/ 10	
8	Homework of HLS		Face-to-face	06:00	20%	5 / 10	CT03 CE04 CB07 CB08 CE01
10	Homework of Hardware Design with Simulink		Face-to-face	04:00	5%	5 / 10	
14	Homework of SystemC		Face-to-face	06:00	20%	5 / 10	
15	Final Exam		No Presential	02:00	50%	5 / 10	CB08 CT03 CE04 CG01 CG03 CB09 CE01 CB07

#### 7.1.2. Final examination

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
3	Homework of Scheduling, Allocation and Binding		No Presential	04:00	5%	/ 10	
8	Homework of HLS		Face-to-face	06:00	20%	5 / 10	CT03 CE04 CB07 CB08 CE01
10	Homework of Hardware Design with Simulink		Face-to-face	04:00	5%	5 / 10	
14	Homework of SystemC		Face-to-face	06:00	20%	5 / 10	

15	Final Exam		No Presential	02:00	50%	5 / 10	CB08 CT03 CE04 CG01 CG03 CB09 CE01 CB07
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### 7.1.3. Referred (re-sit) examination

No se ha definido la evaluación extraordinaria.

## 7.2. Assessment criteria

This subject will be evaluated based on the following aspects:

1. A homework problem that the students will have to provide and discuss in the class (individual)
2. A practical work implementing Different Algorithms by means of High Level Synthesis Tools (team work)
3. A practical work implementing a simple Algorithm by means of Simulink (team work)
4. A practical work modeling a basic Software / Hardware System with SystemC (team work)
5. A Final Exam covering the whole subject (individual)

## 8. Teaching resources

### 8.1. Teaching resources for the subject

Name	Type	Notes
Papers	Bibliography	
Xilinx Tools (Vivado)	Equipment	
PynQ boards	Equipment	
slides for the classes	Bibliography	