ANX-PR/CL/001-01

LEARNING GUIDE

SUBJECT

93000834 - Engineering Of Systems With Processors

DEGREE PROGRAMME

09AQ - Master Universitario En Ingenieria De Telecomunicacion

ACADEMIC YEAR & SEMESTER

2021/22 - Semester 2

Index

Learning guide

1. Description

1.1. Subject details

Name of the subject	93000834 - Engineering Of Systems With Processors
No of credits	6 ECTS
Type	Optional
Academic year ot the programme	Second year
Semester of tuition	Semester 4
Tuition period	February-June
Tuition languages	English
Degree programme	09AQ - Master Universitario en Ingenieria de Telecomunicacion
Centre	09 - Escuela Tecnica Superior De Ingenieros De Telecomunicacion
Academic year	2021-22

2. Faculty

2.1. Faculty members with subject teaching role

Name and surname	Office/Room	Email	Tutoring hours *
Pedro Jose Malagon Marzo (Subject coordinator)	B-113	pedro.malagon.marzo@upm.es	W - 13:00 - 14:00

* The tutoring schedule is indicative and subject to possible changes. Please check tutoring times with the faculty member in charge.

3. Prior knowledge recommended to take the subject

3.1. Recommended (passed) subjects

The subject - recommended (passed), are not defined.

3.2. Other recommended learning outcomes

- Basic knowledge on embedded systems

- Basic programming skills

- Basic knowledge on Processor Architecture

- Basic knowledge on Hardware Description Languages (HDL)

- Basic knowledge on GNU/Linux operating system

4. Skills and learning outcomes *

4.1. Skills to be learned

CE11 - Conocimiento de los lenguajes de descripción hardware para circuitos de alta complejidad.

CE12 - Capacidad para utilizar dispositivos lógicos programables, así como para diseñar sistemas electrónicos avanzados, tanto analógicos como digitales. Capacidad para diseñar componentes de comunicaciones como por ejemplo encaminadores, conmutadores, concentradores, emisores y receptores en diferentes bandas.

CG4 - Que los estudiantes sepan comunicar sus conclusiones ?y los conocimientos y razones últimas que las sustentan? a públicos especializados y no especializados de un modo claro y sin ambigüedades.

4.2. Learning outcomes

RA298 - To describe the design of systems based on microprocessor using block diagrams

RA299 - To implement and use software, memory addressing modes and instructions of advanced processors

RA301 - To design and develop input/output and peripherals of an advanced processor

RA302 - To design and implement new modules in FPGA using HDL

RA304 - To design and implement real world applications using hardware platforms based on advanced processors

RA300 - To specify the software design process for embedded system programming

RA297 - To understand the design of a CPU and the memory unit of an advanced microprocessor

RA296 - To analyse and define advanced processor architectures, coding and programming models

RA303 - To implement applications using a Real-Time operating system running on an advanced processor

* The Learning Guides should reflect the Skills and Learning Outcomes in the same way as indicated in the Degree Verification Memory. For this reason, they have not been translated into English and appear in Spanish.

5. Brief description of the subject and syllabus

5.1. Brief description of the subject

This course provides the required resources to design and develop complex embedded systems, as well as to improve the designs of these processor-based systems. It allows the students to understand and use advanced design concepts in embedded systems using a programmable System-on-Chip: memory system, controllers, peripherals, operating systems, etc. In addition, it allows designing with restrictions such as consumption, cost, reliability or security.

5.2. Syllabus

1. Advanced Processors Architecture: ARM9 with programmable logic

2. Memory Systems: Interfacing memory and DMA

3. Peripherals and controllers: inserting, controlling and debugging AXI IP cores

4. FPGAs: developing and testing custom IP cores

5. HLS: using C++ to generate IP cores

6. Operating Systems: Linux

6. Schedule

6.1. Subject schedule*

Week	Face-to-face classroom activities	Face-to-face laboratory activities	Distant / On-line	Assessment activities
1	**Advanced Processor Architectures** Duration: 02:00 Lecture	**Lab: simple processors** Duration: 02:00 Laboratory assignments		
2	**Memory Systems** Duration: 02:00 Lecture	**Lab: Memory Systems** Duration: 02:00 Laboratory assignments		**Lab evaluation** Problem-solving test Continuous assessment Not Presential Duration: 00:00
3	**Peripherals and controllers** Duration: 02:00 Lecture	**Lab: Peripherals and controllers** Duration: 02:00 Laboratory assignments		**Lab evaluation** Other assessment Continuous assessment Not Presential Duration: 00:00
4	**FPGAs** Duration: 02:00 Lecture	**Lab: HDL design on FPGAs** Duration: 02:00 Laboratory assignments		**Lab evaluation** Other assessment Continuous assessment Not Presential Duration: 00:00
5	**HLS: hardware designed from C++** Duration: 02:00 Lecture	**Lab: hardware designed from C++** Duration: 02:00 Laboratory assignments		**Lab evaluation** Other assessment Continuous assessment Not Presential Duration: 00:00
6	**Operating Systems: Linux** Duration: 02:00 Lecture	**Lab: Operating Systems: Linux** Duration: 02:00 Laboratory assignments		**Lab evaluation** Other assessment Continuous assessment Not Presential Duration: 00:00
7	**Operating Systems: Linux** Duration: 02:00 Lecture	**Lab: Operating Systems: Linux** Duration: 02:00 Laboratory assignments		**Lab evaluation** Other assessment Continuous assessment Not Presential Duration: 00:00
8		**Lab: Final project development** Duration: 04:00 Laboratory assignments		**Lab evaluation** Other assessment Continuous assessment Not Presential Duration: 00:00
9		**Lab: Final project development** Duration: 04:00 Laboratory assignments		

10		**Lab: Final project development** Duration: 04:00 Laboratory assignments		
11		**Lab: Final project development** Duration: 04:00 Laboratory assignments		
12		**Lab: Final project development** Duration: 04:00 Laboratory assignments		
13		**Lab: Final project development** Duration: 04:00 Laboratory assignments		
14		**Lab: Final project development** Duration: 04:00 Laboratory assignments		
15		**Final project: integration** Duration: 04:00 Additional activities		**Exposition of the final project** Group presentation Continuous assessment Presential Duration: 02:00 **Theory test/final project** Written test Final examination Presential Duration: 02:00
16				
17				

Depending on the programme study plan, total values will be calculated according to the ECTS credit unit as 26/27 hours of student face-to-face contact and independent study time.

* The schedule is based on an a priori planning of the subject; it might be modified during the academic year, especially considering the COVID19 evolution.

7. Activities and assessment criteria

7.1. Assessment activities

7.1.1. Continuous assessment

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
2	Lab evaluation	Problem-solving test	No Presential	00:00	10%	/ 10	CE12
3	Lab evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE11
4	Lab evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE12 CE11
5	Lab evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE12 CE11
6	Lab evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE12 CE11
7	Lab evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE12 CE11
8	Lab evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE12 CE11
15	Exposition of the final project	Group presentation	Face-to-face	02:00	30%	5 / 10	CG4

7.1.2. Final examination

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
15	Theory test/final project	Written test	Face-to-face	02:00	100%	5 / 10	CG4 CE12 CE11

7.1.3. Referred (re-sit) examination

Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
Thery test/final project	Written test	Face-to-face	02:00	100%	5 / 10	CG4 CE12 CE11

7.2. Assessment criteria

Considering that the lab exercises are fragments of a whole, which is the final project, the evaluation will be done based on passing the previously defined test.

In the exposition the capacity of communication, technical debate and synthesis will be evaluated.

In compliance with the Evaluation Regulations of the Universidad Politecnica de Madrid, students can be evaluated by a final exam if the notify the coordinator of this course before April 20th. This option implies renouncing to the continuous assesment. The final exam includes presenting the results of a proposed final project and a theory test covering the topics of this course.

8. Teaching resources

8.1. Teaching resources for the subject

Name	Type	Notes
Main Book	Bibliography	Pong P. Chu, "RTL hardware design using VHDL", John Wiley & Sons, 2006
Complementary Book	Bibliography	Tammy Noergaard, "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", 2nd edition, Newnes, 2013
Web pages	Web resource	Scientific papers and relevant industry documentation linked in the moodle web page of this course

9. Other information

9.1. Other information about the subject

The course uses the platform Zybo and the Vivado HLx Design Suite.

The students select the topic of the project. In order to offer them relevant topics, the course introduces the following SDG (Sustainable Development Goals):

- SDG 3: Health:

* 3.6 By 2020, halve the number of global deaths and injuries from road traffic accidents.

- SDG 6: Clean Water and Sanitation

6.6 By 2020, protect and restore water-related ecosystems, including mountains, forests, wetlands, rivers, aquifers and lakes

- SDG 9: Industries, Innovation and Infrastructure

9.4 By 2030, upgrade infrastructure and retrofit industries to make them sustainable, with increased resource-use efficiency and greater adoption of clean and environmentally sound technologies and industrial processes, with all countries taking action in accordance with their respective capabilities

- SDG 11: Cities:

* 11.6 By 2030, reduce the adverse per capita environmental impact of cities, including by paying special attention to air quality and municipal and other waste management