ANX-PR/CL/001-01

LEARNING GUIDE

SUBJECT

93000834 - Engineering Of Systems With Processors

DEGREE PROGRAMME

09AQ - Master Universitario En Ingenieria De Telecomunicacion

ACADEMIC YEAR & SEMESTER

2023/24 - Semester 2

Index

Learning guide

1. Description

1.1. Subject details

Name of the subject	93000834 - Engineering Of Systems With Processors
No of credits	6 ECTS
Type	Optional
Academic year ot the programme	Second year
Semester of tuition	Semester 4
Tuition period	February-June
Tuition languages	English
Degree programme	09AQ - Master Universitario en Ingenieria de Telecomunicacion
Centre	09 - Escuela Tecnica Superior De Ingenieros De Telecomunicacion
Academic year	2023-24

2. Faculty

2.1. Faculty members with subject teaching role

Name and surname	Office/Room	Email	Tutoring hours *
Pedro Jose Malagon Marzo (Subject coordinator)	B-113	pedro.malagon.marzo@upm.es	W - 13:00 - 14:00

* The tutoring schedule is indicative and subject to possible changes. Please check tutoring times with the faculty member in charge.

3. Prior knowledge recommended to take the subject

3.1. Recommended (passed) subjects

The subject - recommended (passed), are not defined.

3.2. Other recommended learning outcomes

- Basic programming skills

- Basic knowledge on embedded systems

- Basic knowledge on Processor Architecture

- Basic knowledge on Hardware Description Languages (HDL)

- Basic knowledge on GNU/Linux operating system

4. Skills and learning outcomes *

4.1. Skills to be learned

CE11 - Conocimiento de los lenguajes de descripción hardware para circuitos de alta complejidad.

CE12 - Capacidad para utilizar dispositivos lógicos programables, así como para diseñar sistemas electrónicos avanzados, tanto analógicos como digitales. Capacidad para diseñar componentes de comunicaciones como por ejemplo encaminadores, conmutadores, concentradores, emisores y receptores en diferentes bandas.

CG4 - Que los estudiantes sepan comunicar sus conclusiones ?y los conocimientos y razones últimas que las sustentan? a públicos especializados y no especializados de un modo claro y sin ambigüedades.

4.2. Learning outcomes

RA298 - To describe the design of systems based on microprocessor using block diagrams

RA301 - To design and develop input/output and peripherals of an advanced processor

RA299 - To implement and use software, memory addressing modes and instructions of advanced processors

RA302 - To design and implement new modules in FPGA using HDL

RA304 - To design and implement real world applications using hardware platforms based on advanced processors

RA300 - To specify the software design process for embedded system programming

RA297 - To understand the design of a CPU and the memory unit of an advanced microprocessor

RA296 - To analyse and define advanced processor architectures, coding and programming models

RA303 - To implement applications using a Real-Time operating system running on an advanced processor

* The Learning Guides should reflect the Skills and Learning Outcomes in the same way as indicated in the Degree Verification Memory. For this reason, they have not been translated into English and appear in Spanish.

5. Brief description of the subject and syllabus

5.1. Brief description of the subject

This course provides the required resources to design and develop complex embedded systems, as well as to improve the designs of these processor-based systems.

It allows the students to understand and use advanced design concepts in embedded systems using a programmable System-on-Chip: memory system, controllers, peripherals, operating systems, etc. In addition, it allows designing with restrictions such as consumption, cost, reliability or security.

5.2. Syllabus

1. Advanced Processors Architecture: ARM9 with programmable logic

2. Operating Systems: Linux

3. Peripherals and controllers: inserting, controlling, simulating and debugging AXI IP cores

4. Memory Systems: Interfacing memory and DMA

5. HLS: using C++ to generate IP cores

6. Schedule

6.1. Subject schedule*

Week	Classroom activities	Laboratory activities	Distant / On-line	Assessment activities
1	**Advanced Processor Architectures** Duration: 02:00 Lecture	**Tutorial 1: Microcontroller and IDE** Duration: 02:00 Laboratory assignments		
2	**Operating Systems: Linux** Duration: 02:00 Lecture	**Tutorial 2: Linux in Embedded Systems** Duration: 02:00 Laboratory assignments		
3	**Peripherals and controllers** Duration: 01:30 Lecture	**Tutorial 3: AXI Bus. Peripherals and debugging in FPGA-based SoC** Duration: 02:30 Laboratory assignments		
4	**Operating Systems: Drivers in Linux** Duration: 02:00 Lecture	**Tutorial 4: Drivers in Linux in Embedded Systems** Duration: 02:00 Laboratory assignments		
5		**Exercise 1: Web-based LED controller** Duration: 04:00 Laboratory assignments		
6	**Memory Systems and Data Movement** Duration: 02:00 Lecture	**Tutorial 5: Memory Systems and data movement** Duration: 02:00 Laboratory assignments		
7		**Exercise 2: Audio/Analog continuous sampling data with DMA** Duration: 04:00 Laboratory assignments		
8	**Embedded Systems: profiling** Duration: 01:00 Lecture	**Exercise 2: Audio/Analog continuous sampling data with DMA** Duration: 01:00 Laboratory assignments **Tutorial 6: profiling** Duration: 02:00 Laboratory assignments		
9	**HLS: hardware designed from C++** Duration: 02:00 Lecture	**Tutorial 7: matrix multiplicator with HLS** Duration: 02:00 Laboratory assignments		
10	**HLS: integrating custom IP blocks in SoC** Duration: 02:00 Lecture	**Tutorial 8: HLS FIR filter with audio** Duration: 02:00 Laboratory assignments		
11		**Exercise 3: LED Matrix Controller in HLS** Duration: 04:00 Laboratory assignments		

12	**HLS: optimizing hardware designed from C++ for DSP** Duration: 02:00 Lecture	**Tutorial 9: Optimizing Pipelining and Dataflow in HLS** Duration: 01:00 Laboratory assignments **Tutorial 9: Optimizing memory arrangement in HLS** Duration: 01:00 Laboratory assignments		
13	**Filtering** Duration: 01:00 Lecture	**Exercise 4: IIR filter and Energy calculation in HW and SW** Duration: 03:00 Laboratory assignments		
14		**Exercise 4: IIR filter and energy calculation in HW and SW** Duration: 04:00 Laboratory assignments		
15		**Project: Integration of exercises** Duration: 04:00 Laboratory assignments		
16		**Project: Integration of exercises** Duration: 04:00 Laboratory assignments		
17				**Tutorial evaluation** Other assessment Continuous assessment and final examination Not Presential Duration: 00:00 **Dissertation on tutorials and exercises** Problem-solving test Continuous assessment and final examination Presential Duration: 00:30 **Exercise 1 evaluation** Other assessment Continuous assessment and final examination Not Presential Duration: 00:00 **Exercise 2 evaluation** Other assessment Continuous assessment and final examination Not Presential Duration: 00:00 **Exercise 3 evaluation** Other assessment Continuous assessment and final examination Not Presential Duration: 00:00 **Exercise 4 evaluation** Other assessment Continuous assessment and final examination

				Not Presential Duration: 00:00 **Exercise integration** Other assessment Continuous assessment and final examination Not Presential Duration: 00:00

Depending on the programme study plan, total values will be calculated according to the ECTS credit unit as 26/27 hours of student face-to-face contact and independent study time.

* The schedule is based on an a priori planning of the subject; it might be modified during the academic year, especially considering the COVID19 evolution.

7. Activities and assessment criteria

7.1. Assessment activities

7.1.1. Assessment

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
17	Tutorial evaluation	Other assessment	No Presential	00:00	40%	/ 10	CE12 CE11
17	Dissertation on tutorials and exercises	Problem-solving test	Face-to-face	00:30	10%	5 / 10	CG4
17	Exercise 1 evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE12
17	Exercise 2 evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE12
17	Exercise 3 evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE11
17	Exercise 4 evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE12 CE11
17	Exercise integration	Other assessment	No Presential	00:00	10%	/ 10	CE12 CE11

7.1.2. Global examination

Week	Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
17	Tutorial evaluation	Other assessment	No Presential	00:00	40%	/ 10	CE12 CE11
17	Dissertation on tutorials and exercises	Problem-solving test	Face-to-face	00:30	10%	5 / 10	CG4
17	Exercise 1 evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE12
17	Exercise 2 evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE12
17	Exercise 3 evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE11
17	Exercise 4 evaluation	Other assessment	No Presential	00:00	10%	/ 10	CE12 CE11

17	Exercise integration	Other assessment	No Presential	00:00	10%	/ 10	CE12 CE11

7.1.3. Referred (re-sit) examination

Description	Modality	Type	Duration	Weight	Minimum grade	Evaluated skills
Tutorial evaluation and dissertation	Problem-solving test	Face-to-face	00:30	50%	5 / 10	CG4 CE12 CE11
Exercise evaluation and dissertation	Problem-solving test	Face-to-face	00:30	50%	/ 10	CG4 CE12 CE11

7.2. Assessment criteria

The course is full of practical exercises. Some of them are very guided (tutorials) and some of them are not so guided, so the student must apply what has been learnt in the tutorials to the exercises.

The tutorials and exercises are interleaved along the semester.

Fully completing the tutorials represents 40% of the subject evaluation, and it would be enough to succesfully complete the subject.

The tutorials are evaluated as they are finished and uploaded to a repository.

Students are free to complete the tutorials up to the exam date.

There are 4 exercises, each representing a 10% of the subject final grade, and an integration exercise to build a project from the individual exercises, which also represent a 10%.

The exercises are evaluated as they are finished and uploaded to a repository.

Students are free to complete the exercises up to the exam date.

The exam consists on an oral dissertation (interview) on the tutorials and exercises, to check that the student has understood the basics of the subject.

Alternatively, Students can propose a project to be implemented with similar characteristics of what it is seen, using a Zynq-based or equivalent platform, with software running on the embedded processor, HLS based components and the use of AXI buses to interconnect them.

The project must be previously approved by the teacher. In this case, the project would represent 100% of the final grade with a final dissertation (interview) on the project.

8. Teaching resources

8.1. Teaching resources for the subject

Name	Type	Notes
Web pages	Web resource	Scientific papers and relevant industry documentation linked in the moodle web page of this course
Main Book	Bibliography	Pong P. Chu, "RTL hardware design using VHDL", John Wiley & Sons, 2006
Complementary Book	Bibliography	Tammy Noergaard, "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", 2nd edition, Newnes, 2013

9. Other information

9.1. Other information about the subject

The course uses the platform Zybo and the Vivado HLx Design Suite, which enables to reuse the platform to implement complex HW/SW systems, updating the system to increase lifecycle of HW platforms using reconfigurable systems

The students select the topic of the project. In order to offer them relevant topics, the course introduces the following SDG (Sustainable Development Goals):

9.4 By 2030, upgrade infrastructure and retrofit industries to make them sustainable, with increased resource-use efficiency and greater adoption of clean and environmentally sound technologies and industrial processes, with all countries taking action in accordance with their respective capabilities